

Aspects of Next-Generation Parallel Computers

- *Experience with CP-PACS*
- *How much more?*
- *How?*

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CP-PACS

- Machine specifications:
 - 2048PU+128IOU
 - 614GFLOPS peak
 - 64+256GByte memory
 - 1058GByte disk
- Operation:
 - full operation started in October 1996
 - *already 3 years ago.....*



Lattice QCD Projects on CP-PACS

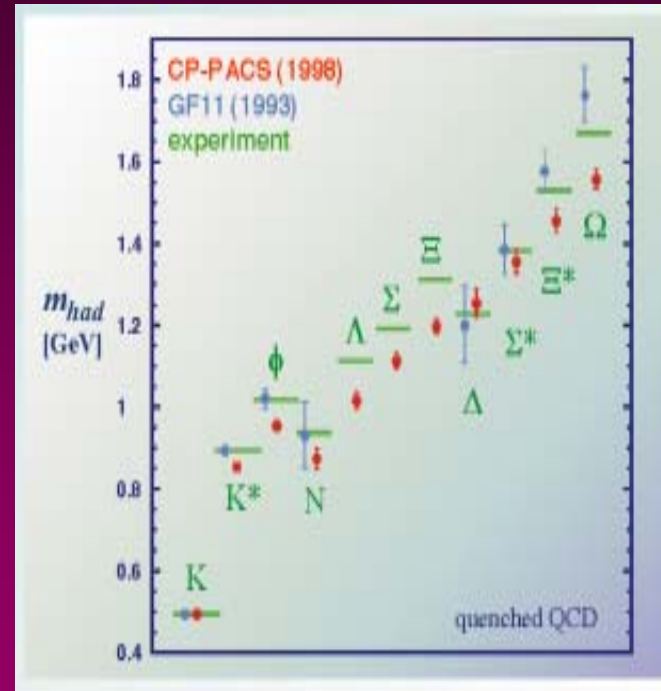
- The first year: October 1996 - October 1997
Quenched light hadron spectrum
- The next two years: September 1997 - present
Two-flavor full QCD

CP-PACS Performance (ratio to peak):

50% for quenched run	$64^3 \times 112$	2048PU
34% for full QCD	$24^3 \times 48$	512PU

Quenched Light Hadron Spectrum

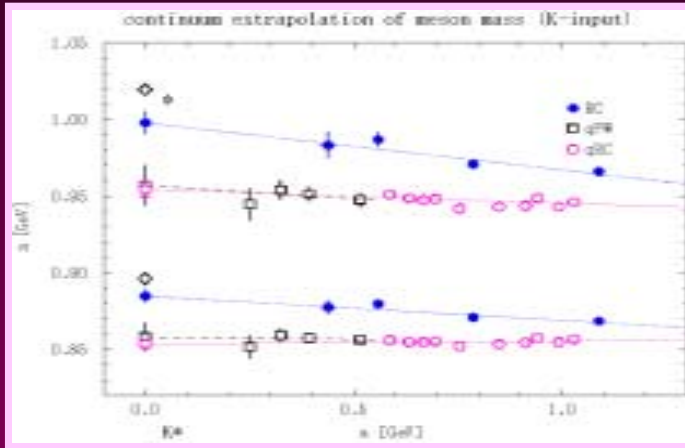
- concentrated effort to pin down the quenched spectrum
- could borrow on accumulated wisdom from previous studies



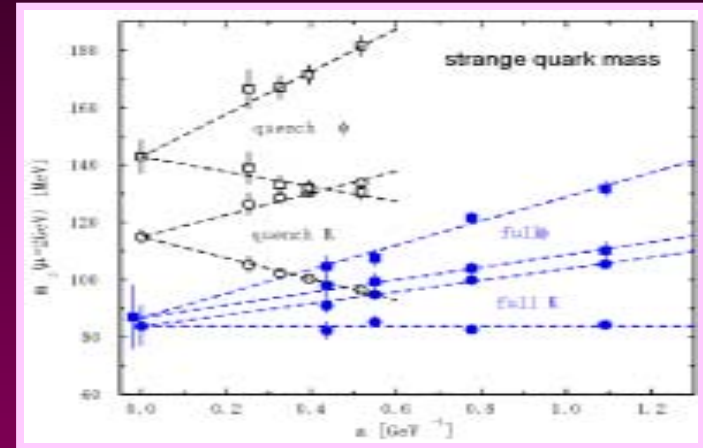
- *clear observation of quenching effects*

Selected Two-Flavor Results

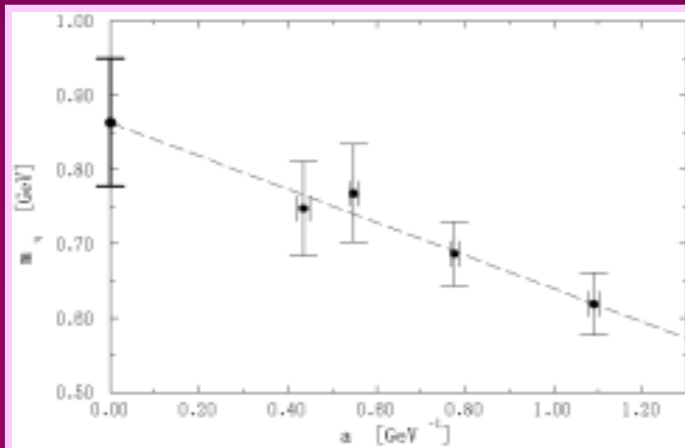
Meson hyperfine splitting



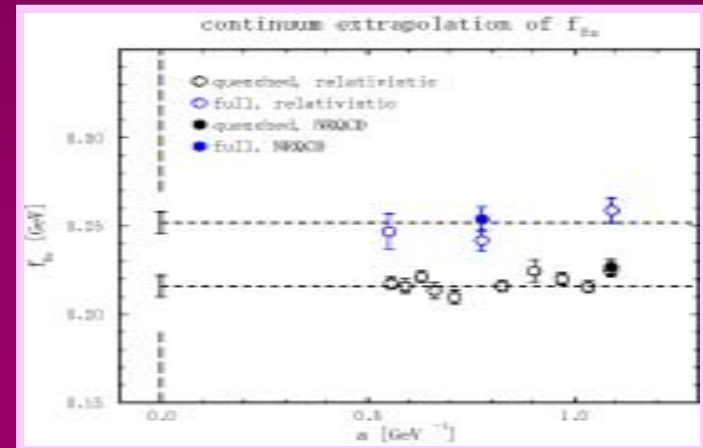
Strange quark mass



Eta meson mass



B meson decay constant



Two-Flavor Full QCD

- multi-faceted attempt toward realistic simulation of QCD examining
 - light to heavy quarks
 - spectra to matrix elements
 - zero to high temperatures
- largely unexplored territory in spite of many attempts since middle of 80's
- more trial & errors involved
- *several encouraging results emerging showing importance of sea quark effects*

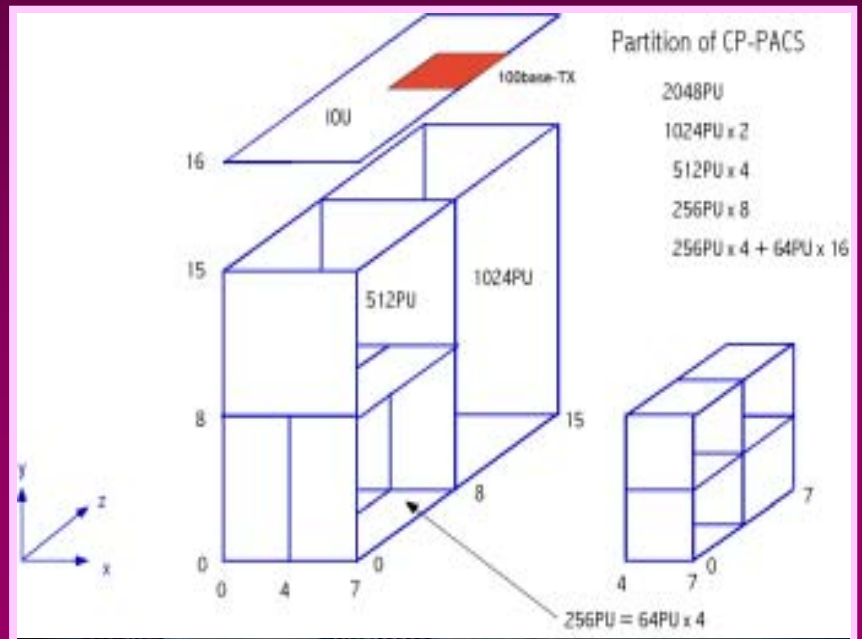
Partitioned use of CP-PACS

- Quenched light hadron spectrum

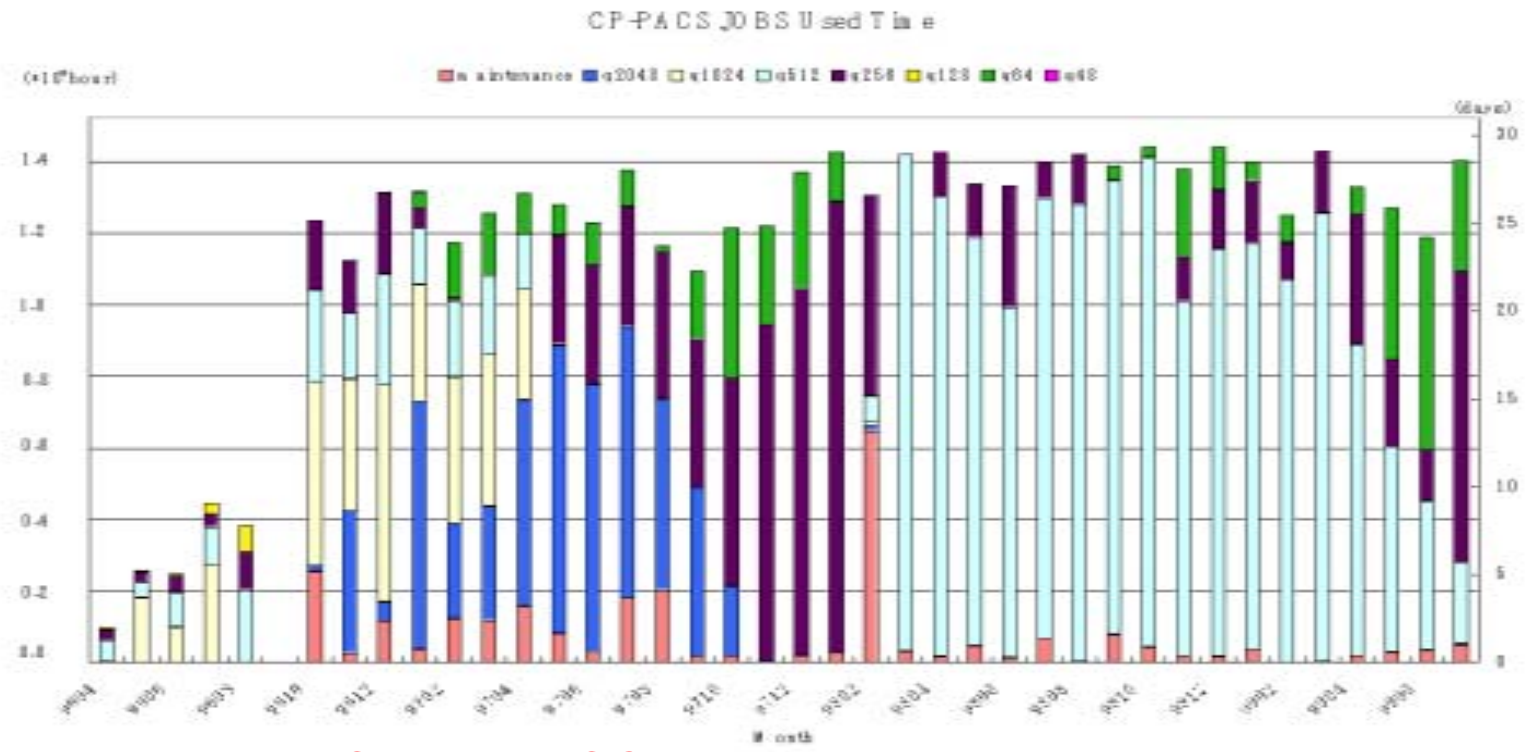
- $32^3 \times 56$ 256PU
- $40^3 \times 70$ 512PU
- $48^3 \times 84$ 1024PU
- $64^3 \times 112$ 2048PU

- Two-flavor full QCD

- $12^3 \times 24$ 64PU
- $16^3 \times 32$ 256PU
- $24^3 \times 48$ 512PU



Monthly CPU time usage of CP-PACS



Quenched QCD

Full QCD



Impact of the Two Projects - personal view

-

- *have manifested the limitation of quenched QCD*
by explicitly showing the discrepancy
- *have ushered in the era of full QCD*
by explicitly finding sea quark effects
- *future is in full QCD*

Next Step of Lattice QCD

- Realistic dynamical quark spectrum,
i.e., 2 (*up & down*) + 1 (*strange*)
- Lighter *up & down* quarks,
i.e., $\pi/\rho=0.6 \rightarrow 0.4$
- Larger spatial size,
i.e., $L=2.4 \text{ fm} \rightarrow 3.0 \text{ fm}$
- Better chiral behavior
use of domain wall/overlap formalism

An Estimate of CPU Time:method

Assumptions

- RG -gauge + clover quark for 2 dynamical flavors
- HMC algorithm
- BiCGStab solver

FLOP analysis

$$FLOP = (A + B \cdot N_{inv}) \frac{V}{\Delta\tau} \times 10^{-12} \text{ TFLOPS} \cdot \text{sec/trajectory}$$

CP-PACS experience

- A = 45600, B=8800
- $N_{inv} = 31 + 10.7/mq$
- $Dt = (0.223mq - 0.620mq^2) \times 24/L$ (mq in GeV)

similar analysis for communication

An Estimate of CPU Time: Results

physical system	target	current
<ul style="list-style-type: none">• physical size	3 fm	2.5fm
<ul style="list-style-type: none">• quark mass	15 MeV (pi/rho=0.4)	44 MeV (0.6)
<ul style="list-style-type: none">• #trajectory	25000	2000

simulation	conventional	domain wall
<ul style="list-style-type: none">• lattice spacing	3 GeV	2 GeV
<ul style="list-style-type: none">• lattice size	48³ x 96	32³ x 64 x 10
<ul style="list-style-type: none">• CPU time	409 days	343 days
<ul style="list-style-type: none">• ratio of commun.	25%	20%

machine parameters:

- **32Gflops/PU , 16³ = 4096PU**
- **131 Tflops total**
- **16GBvte/sec/channel**

O(100Tflops) needed

Road to O(100Tflops)

- full QCD to everyone's satisfaction will require O(100Tflops)
- similar requirement from many other fields in computational science and engineering
- When will it become technologically feasible?
- What are the architectural issues?

Advance of Processor Technology

SIA roadmap on semiconductor technology

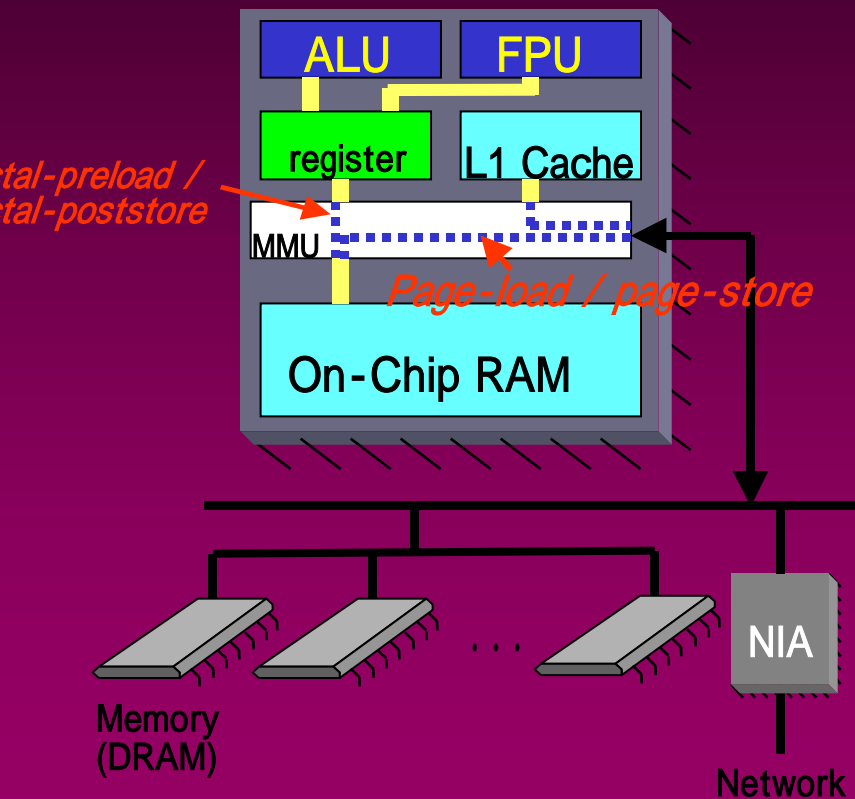
Year	1999	2001	2003	2006	2009	2012
rule (um)	0.18	0.15	0.13	0.10	0.07	0.05
clock(MHz)	1250	1500	2100	3500	6000	10000
tr. in MPU	21M	40M	76M	200M	520M	1.4B
power(W)	90	110	130	160	170	175

- 2GHz clock / 4 pipelines of add&mult = 16Gflops
not a dream around 2003

e.g. Earth Simulator (2001)

- 8Gflops vector CPU x 8 = 64 Gflops / node
- 64 Gflops x 640 nodes = 40Tflops

Processor with on-chip Memory



- FPU's will be running much faster than data can be fed from off-chip memory
- use *SRAM memory on-chip* to secure the bandwidth (data repeatedly used are kept on-chip in a controlled way)

Research for the Future Program (JSPS) at CCP

R&D of key technologies for next-generation MPP

- processor architecture with memory on-chip
- parallel I/O and visualization

Research for the Future Program (RFTF*)

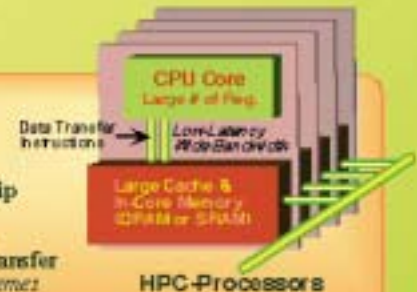
*Challenge to the New Generation
High Performance Parallel Processing*

New Generation Processor Architecture

Utilization of Very Large number of Transistors on Chip
More floating point registers & function units

Combination of Logic/Memory on Chip
High-throughput/Low-latency data transfer

Advanced Instruction Set for Data Transfer
Combination of Preload/Prefetch schemes

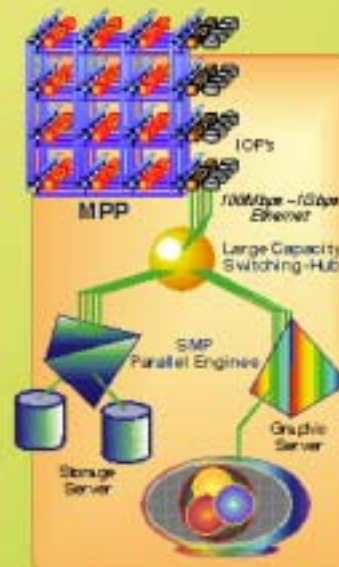


Parallel Input/Output Channel based on Commodity Resources

Utilization of Large Number of I/O Processors in MPP
Wide-bandwidth communication with outer environment

Commodity Based Network
Good cost/performance in communication & flexibility for various platforms

User Friendly API
High usability and programmability



Parallel Visualization

Parallelization of De facto Standard Visualization Libraries
High portability (AVS, X11, etc.)

Spatial and Functional Parallelization
Data domain decomposition & function pipelining

High-Bandwidth based on Parallel I/O
High-bandwidth real time visualization

*This program is supported by Japan Society for the Promotion of Science (JSPS).

Conclusions

- *O(1 Tflops) turned out sufficient to yield convincing results for quenched QCD and first systematic results of sea quark effects in full QCD*
- *probably time to start thinking seriously about O(100 Tflops) which will be required for convincing results in full QCD*