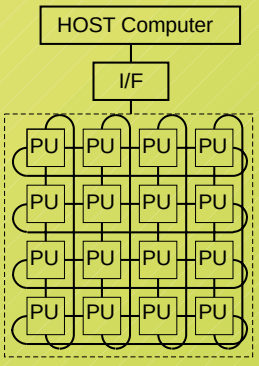
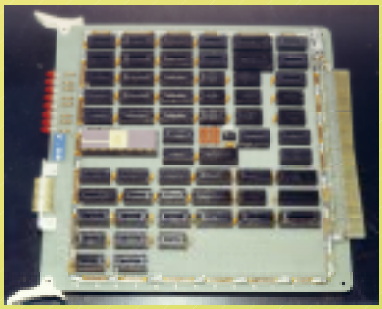
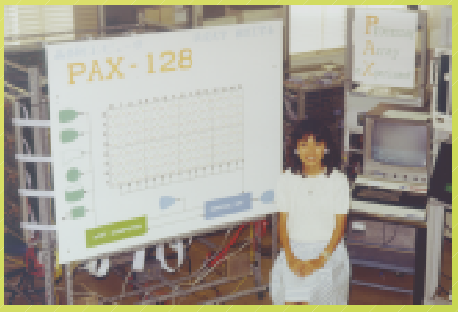
History of PACS/PAX Computers

Since 1977, a series of parallel computers have been constructed by T. Hoshino, T. Kawai and collaborators, adopting a 2D-torus network as the basic architecture. CP-PACS is an extension of this project. Currently, QCDPAX and CP-PACS are in operation for large-scale physics calculations at the Center for Computational Physics of the University of Tsukuba.





PU board of PACS-9 (1978)



PAX-128 (1983) with control unit

Year	Machine	Performance	#PU	Memory	CPU/MPU
1978	PACS-9	7 KFLOPS	9		M6800
1980	PAX-32	0.5 MFLOPS	32	576 KB	M6800/AM9511
1983	PAX-128	4 MFLOPS	128	3 MB	M68B00/AM9511-4
1984	PAX-32J	3 MFLOPS	32	4 MB	DCJ-11
1989	QCDPAX	14 GFLOPS	480	3 GB	M68020/L64133
1996	CP-PACS	307 GFLOPS	1024	64 GB	extended PA-RISC
1997	CP-PACS	614 GFLOPS	2048	128 GB	1.1

PU array of PAX-32 (1980)

PAX-32J (1984)

A cabinet of QCDPAX (1989)