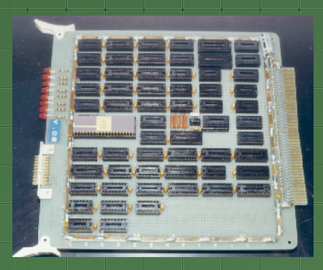
Center for Computational Sciences, University of Tsukuba
http://www.ccs.tsukuba.ac.jp/

Development of Parallel Computers at Tsukuba

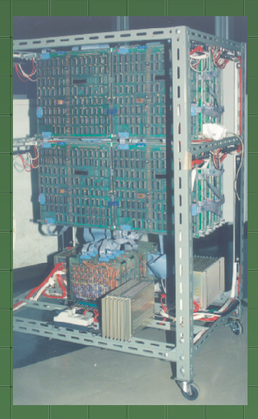
~ from PACS-9 (1978) to CP-PACS (1996) ~

PACS/PAX Computers

University of Tsukuba is one of the pioneering institutes in the development of parallel computers in Japan. In 1997, Tsutomu Hoshino and Toshio Kawai started to constract parallel computers at Tsukuba, adopting two-dimensional torus network as the fundamental architecture. The first computer "PACS-9" was constracted in 1978 and achieved the speed of 7000 operations/sec. Since then, a series of parallel computers have been developed and applied for simulations of physical systems such as the nuclear matter in the reactor.



PACS-9(1978)



PAX-32(1980)

year	machines	#PU	performance	memory
1978	PACS-9	9	7 KFLOPS	
1080	PAX-32	32	0.5 MFLOPS	0.5 MB
1983	PAX-128	128	4 MFLOPS	5 MB
1984	PAX-32J	32	3 MFLOPS	4 MB
1989	QCDPAX	480	14 GFLOPS	3 GB
1996	CP-PACS	2048	614 GFLOPS	128 GB

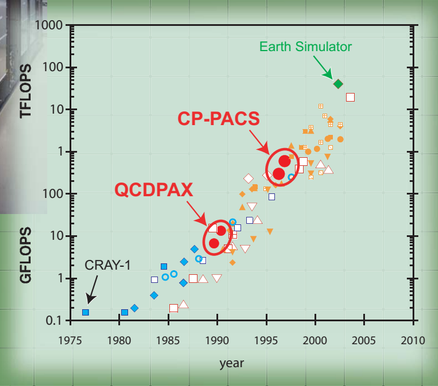
History of PACS/PAX computers

QCDPAX (1989)

QCDPAX, developed in 1989 as the fifth computer of the series, is dedicated for the simulation of Quamtum Chromodynamics, the fundamental theory of quarks. QCDPAX consists of 480 processing units. With the peak speed of 14 GFLOPS, QCDPAX carried out simulations of quarks at zero and finite temperatures.

CP-PACS

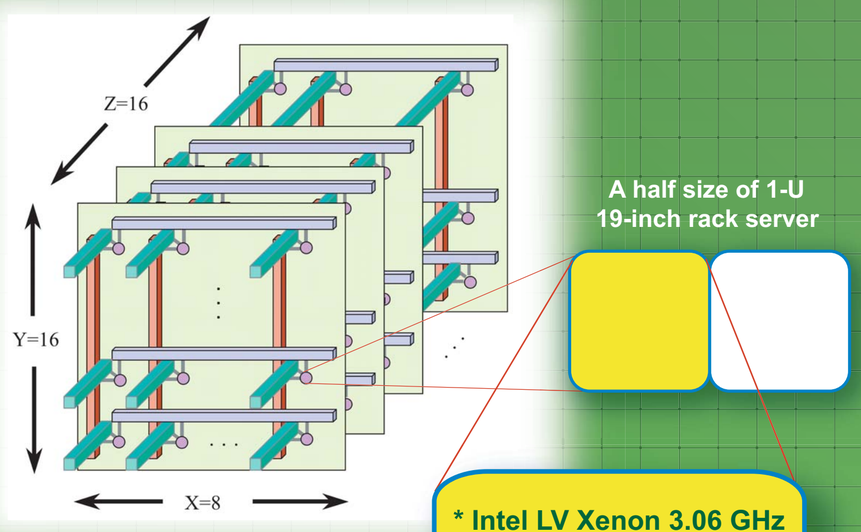
CP-PACS is the sixth of the PACS/PAX parallel computers. With 2048 processing units and 128 I/O nodes interconnected by a three-dimensional hypercrossbar network, CP-PACS achieved the peak speed of 614 GFLOPS and was ranked No.1 in the TOP 500 list for supercomputers in November 1996. CP-PACS has been intensively applied for simulations in the Physics of Fields ranging from quarks to universe.



Development of high performance computers

CP-PACS II

CP-PACS II with 2048 CPU's



CP-PACS II is the seventh generation of the PACS series, a PC-cluster with 2048 CPUs and 12.5 TFLOPS of peak performance. The building block is a specially designed 1-U size board which contains two sets of separated Linux-ready PC without SMP configuration. Since each CPU on the board accesses memory and network interface with full bandwidth, the potential performance is significantly higher than standard dual-CPU SMP servers, albeit keeping the same density. CP-PACS II is also equipped with a specially designed 3-D Hyper-Crossbar Network based on channel-bonding technology of Gigabit Ethernet to provide high bisection bandwidth with low cost.