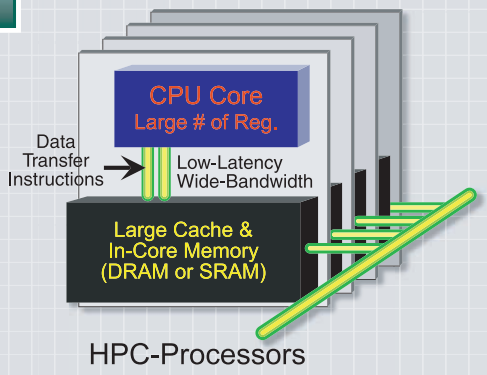
Center for Computational Physics University of Tsukuba

Research for the Future Program (RFTF*)

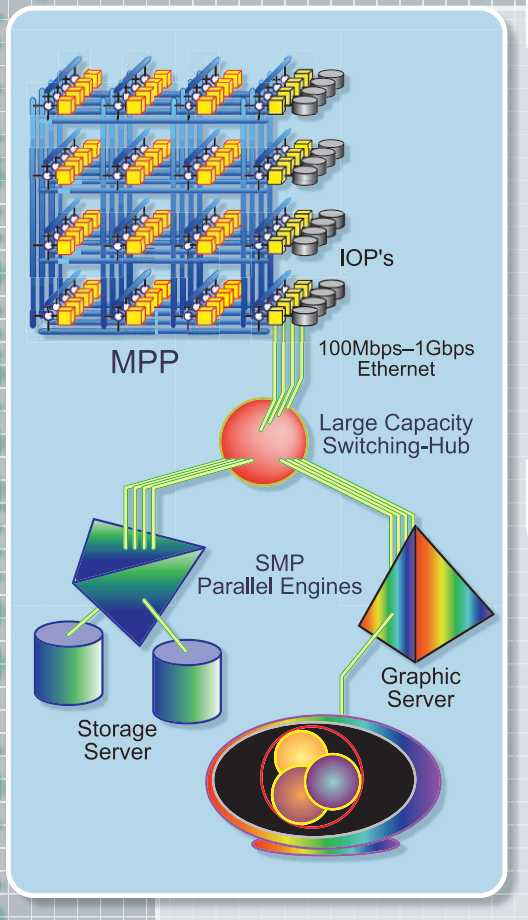
Challenge to the New Generation High Performance Parallel Processing

New Generation Processor Architecture

- **Utilization of Very Large number of Transistors on Chip**
  - More floating point registers & function units
- **Combination of Logic/Memory on Chip**
  - High-throughput/Low-latency data transfer
- **Advanced Instruction Set for Data Transfer**
  - Combination of Preload/Prefetch schemes



HPC-Processors



Parallel Input/Output Channel based on Commodity Resources

- **Utilization of Large Number of I/O Processors in MPP**
  - Wide-bandwidth communication with outer environment
- **Commodity Based Network**
  - Good cost/performance in communication & flexibility for various platforms
- **User Friendly API**
  - High usability and programmability

Parallel Visualization

- **Parallelization of Defacto Standard Visualization Libraries**
  - High portability (AVS, X11, etc.)
- **Spatial and Functional Parallelization**
  - Data domain decomposition & function pipelining
- **High-Bandwidth based on Parallel I/O**
  - High-bandwidth real time visualization

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