

SCIMA

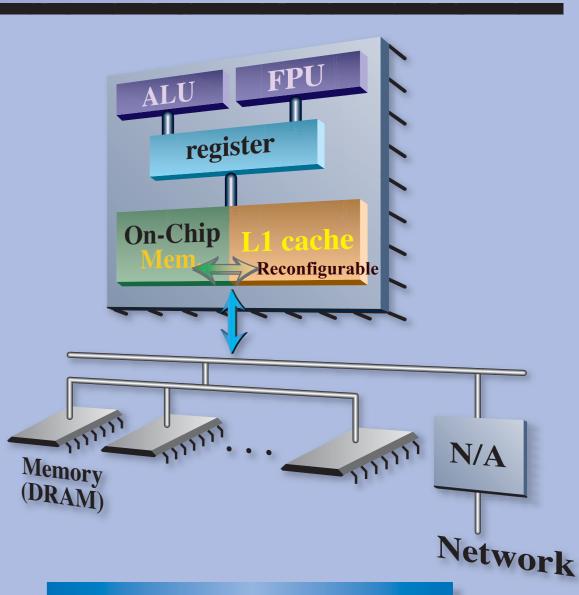
A Software Controlled Integrated Memory Architecture for MegaScale Computing Computing

Objective

- Power Reduction in High-Performance Processors
- Conventional Cache is not good in HPC (Memory Wall Problem)
 - unwilling line conflicts
 - fixed amount of Off-Chip Memory data transfer

Architecture

- Strategy : Software Control
- Addressable On-Chip Memory in addition to conventional cache
 - On-Chip Memory and Cache are reconfiguable
- Reduction of Dynamic / Static Energy Consumption



- fewer bit switching and less on-chip storage
- Explicit data transfer between On-Chip Memory and Off-Chip Memory
 - Reusable array: reserve On-Chip Memory for reuse
 - Not- Reusable array : use On-Chip Memory as stream buffers

Compiler

Compiler Optimization using Hint Information

- reduce programmers' burden
- indicate only the target loop and the array reusability

```
!$scm opt_reusable(x, y, z)
do ii = 1, N, BLK
:
    do i = ii, ii+BLK, 1
        :
        z(i,j) = z(i,j) + x(i,k) * y(k,j)
        enddo
enddo
!$scm opt_end(x,y,z) end of optimization
```

```
!$scm opt_notreusable(x, y)
do i = 1, N
sum = sum + x(i) * y(i)
enddo
!$scm opt_end(x,y) end of optimization
```

Overview of SCIMA

Evaluation Results

